

Roll No.

24324

B. Tech. 6th Semester (CSE)

Examination – May, 2019

DIGITAL SYSTEM DESIGN

Paper : EE-310-F

Time : Three Hours]

[Maximum Marks : 100

Before answering the questions, candidates should ensure that they have been supplied the correct and complete question paper. No complaint in this regard, will be entertained after examination.

Note : Attempt *five* questions in all, selecting *one* question from each Section. Question No. 1 is *compulsory*. All questions carry equal marks.

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|---|---|
| 1. (a) Discuss the different units of VHDL. | 4 |
| (b) Write a VHDL code for Half-adder. | 4 |
| (c) Compare between PLA and PAL. | 4 |
| (d) Differentiate between sequential and concurrent statements. | 4 |

- (e) List out the operator used in VHDL. 4

SECTION – A

2. Discuss the various types of Data objects and data types using in VHDL. 20
3. (a) What is overloading ? Discuss different types of overloading. 10
- (b) Explain the Architecture body with an example. 10

SECTION – B

4. Explain the following statements with an example :

$$4 \times 5 = 20$$

- (a) Process statement
- (b) If-else statement
- (c) Wait statement
- (d) Case statement

5. Write a short note on : 7, 7, 6

- (a) Subprogram
- (b) Package and libraries
- (c) Generic

SECTION – C

6. Write a VHDL code for following :

4 × 5 = 20

- (a) Encoder
- (b) 2 × 4 decoder
- (c) Shift Register
- (d) Comparator

7. (a) Implement the Boolean expression

$$y = AB + A\bar{C} + \bar{B}C.$$

10

(b) Write a structural modeling VHDL code for Full-adder using Half-adder. 10

SECTION – D

8. Write a short note on :

20

- (a) GAL
- (b) CPLD
- (c) PLA

9. (a) Discuss the block diagram of FPGA. Also explain the LUT used in FPGA. 12
- (b) Differentiate between CPLD and FPGA. 8
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